

# **SATA DISK CHIP DESIGN GUIDE**

## Application Note

**August 1, 2011**  
Revision 1.1

*This Application Note Describes the Design Considerations  
for Integrating SATA Disk Chip product*

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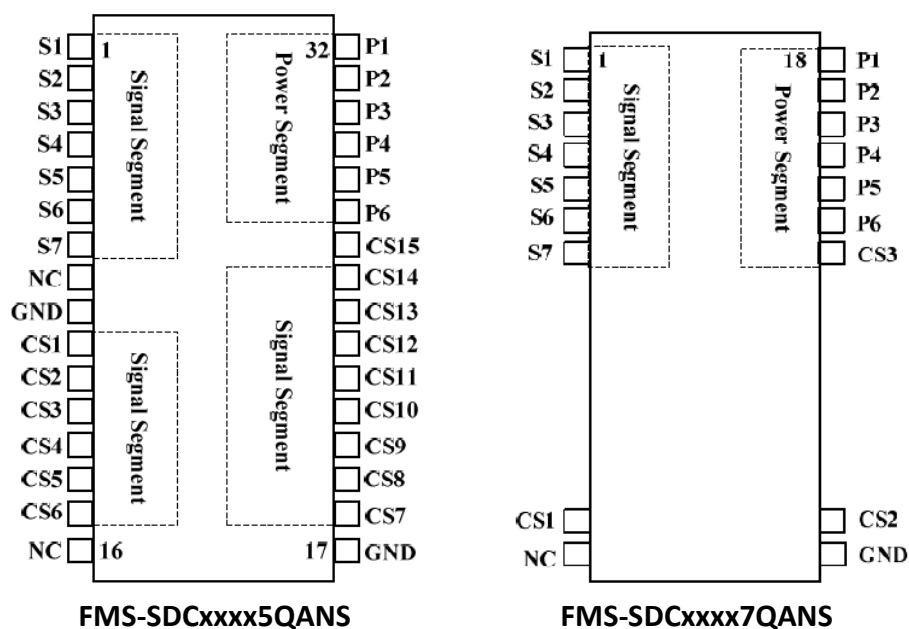
# SATA Disk Chip Design Guide

## Introduction

Fortasa's SATA-Disk Chip (SDC) is an embedded flash system offering exceptional reliability. The SDC consists of a built-Flash controller and Flash memory device(s) packaged in either the standard 32-pin DIP or the 18-pin DIP package for easy, reliable and economical mounting to a system board.

There are two types of connectors for SDC: SDC (FMS-SDCxxx5QANS) with 32-pin and SDC (FMS-SDCxxx7QANS) with 18-pin connector respectively.

### PIN ASSIGNMENTS



## Signal Description

**P1- P6** – Used to connect to power supply of 3.3 volts as the power segment.

**S1 - S7** – This is a bi-directional data bus between the Host System and the SDC.

### For FMS-SDCxxx5QANS

**CS1 - CS5, CS8 - CS14**– Reserved, Do Not Connect

**CS6**– Used to indicate serial ATA physical layer communication.

**CS7**– Used to indicate that SDC is active and usually connected to a LED indicator on the system to report activity.

**CS15**– Used to protect the SDC from being written. When WP# pin is low, the SDC is write-protected to prohibit any inadvertent writes.

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### For FMS-SDCxxx7QANS

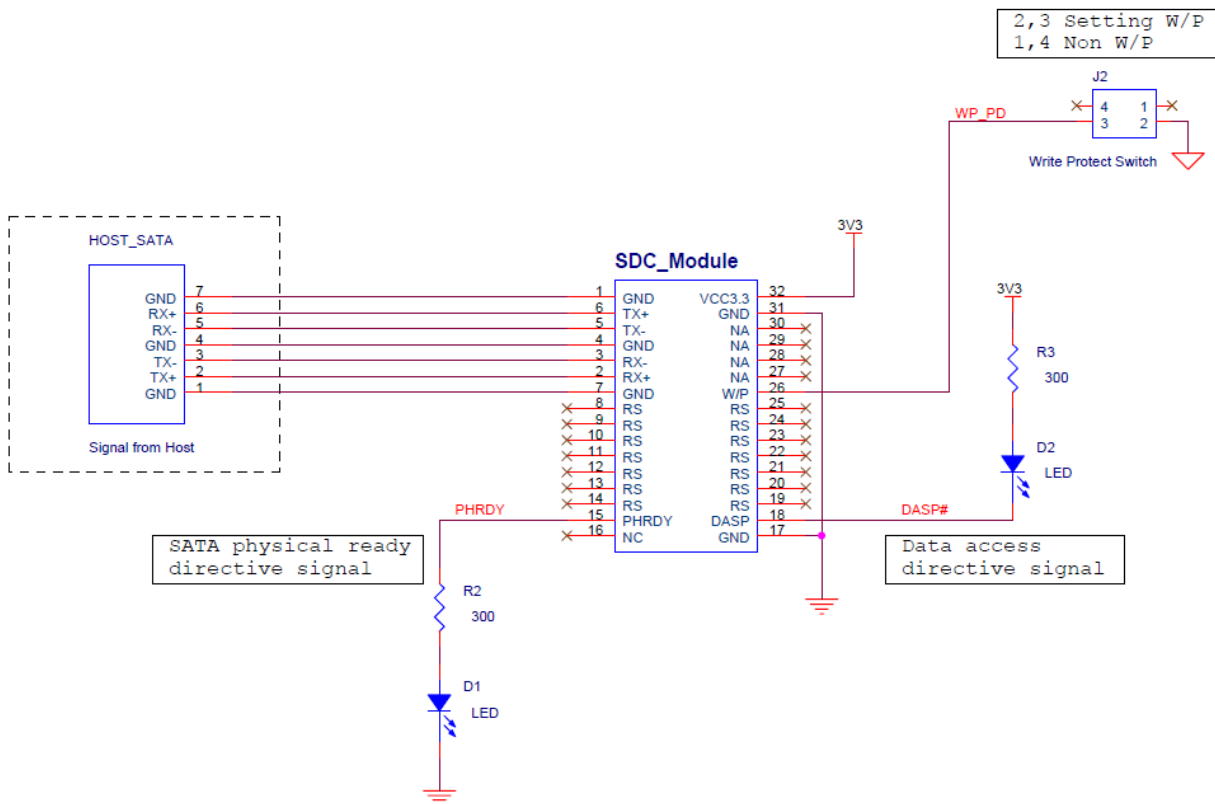
**CS1**– Used to indicate serial ATA physical layer communication.

**CS2**– Used to indicate that SDC is active and usually connected to a LED indicator on the system to report activity.

**CS3**– Used to protect the SDC from being written. When WP# pin is low, the SDC is write-protected to prohibit any inadvertent writes.

## Reference Schematics

### For FMS-SDCxxx5QANS

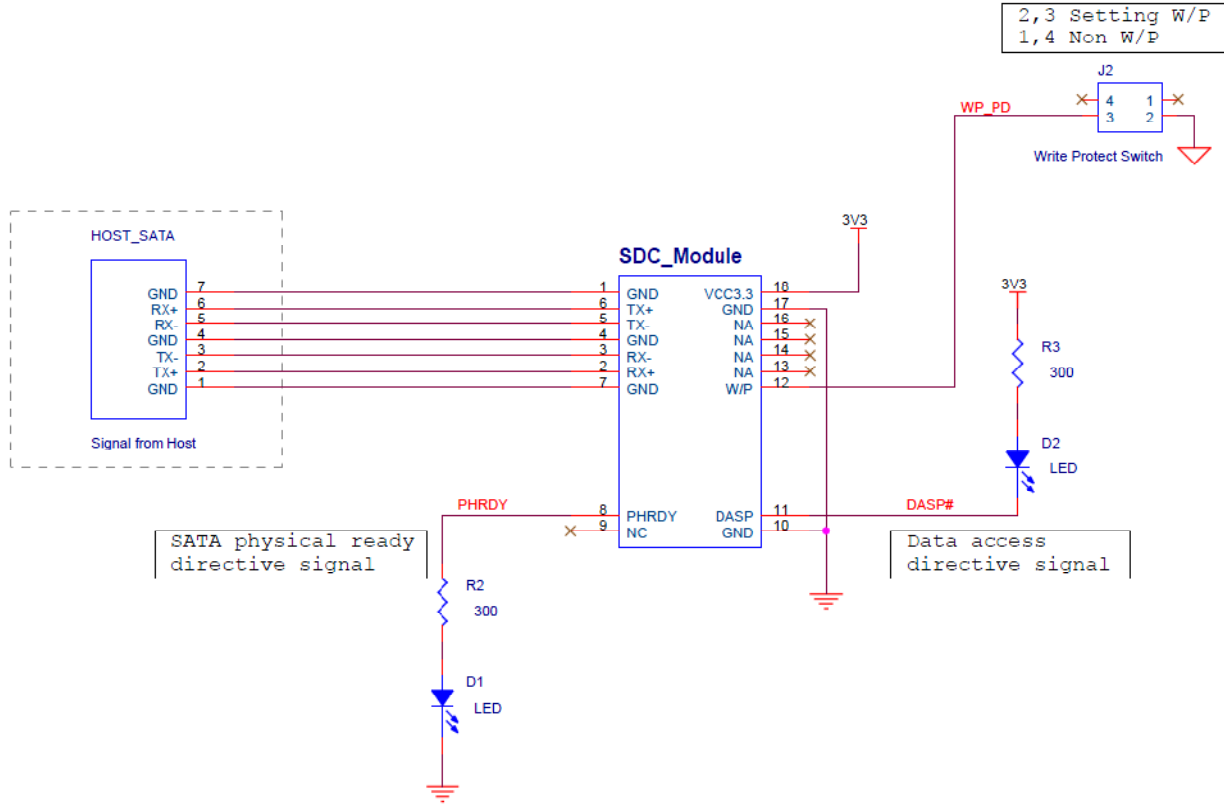


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For FMS-SDCxxx7QANS



### Revision History

Revision	Date	Description	Comments
1.0	2/18/2011	Initial Release	
1.1	8/1/2011	Corrected Reference Schematics	

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