RoHS Compliant

Industrial Embedded MMC Series – e•MMC™

Datasheet for Industrial eMMC 4.51

June 12, 2014
Revision 1.2

This Specification Describes the Features and Capabilities of the Extended Temperature Industrial e•MMC

Please Contact Fortasa Memory Systems Sales for any Custom Features Required For Your Specific Application

4151 Middlefield Road
2nd Floor
Palo Alto, CA 94303 USA
888-367-8588
www.fortasa.com

Features:

- **Packaged NAND flash memory with e•MMC 4.51 interface**
  – Compliant with eMMC Specification Ver. 4.4, 4.41 & 4.5
- **Bus mode**
  - Provides variable clock frequencies of 0-200MHz.
  - Ten-wire bus (clock, 1 bit command, 8 bit data bus) and a hardware reset.
- **Supports three different data bus widths : 1 bit(default), 4 bits, 8 bits**
  - Data transfer rate: up to 52Mbyte/s (using 8 parallel data lines at 52 MHz)
  - Single data rate: up to 200Mbyte/s @ HS200(Host clock @ 200MHz)
  - Dual data rate: up to 104Mbyte/s @ 52MHz
- **Supports (Alternate) Boot Operation Mode to provide a simple boot sequence method**
- **Supports SLEEP/AWAKE (CMD5).**
- **Host initiated explicit sleep mode for power saving**
- **Enhanced Write Protection with Permanent and Partial protection options**
- **Supports Multiple User Data Partition with Enhanced User Data Area options**
- **Supports Background Operations & High Priority Interrupt (HPI)**
- **Supports enhanced storage media feature for better reliability**
- **Error free memory access**
  - Internal error correction code (ECC) to protect data communication
  - Internal enhanced data management algorithm
  - Solid protection of sudden power failure safe-update operations for data content
- **Security**
  - Support secure bad block erase commands
  - Enhanced Write Protection with permanent and partial protection options
- **Capacity**
  – 4, 8, 16, 32GB
- **Low power consumption (typical)**
  – Supply voltage: V_{CCQ} = 1.8V / 3.3V, V_{CC} = 3.3V
  – Active mode: 200 mA
  – Sleep mode: 300 µA
- **NAND flash type: MLC**
- **Performance**
  – Sustained Read: up to 29 MB/sec
  – Sustained write: up to 32 MB/sec
- **Temperature ranges**
  – Operation:
  Standard Temperature: -25℃ to 85℃
  – Storage: -40℃ to 85℃
- **Physical Dimensions**
  – 13mm x 11.5mm x 1.0 mm – 153-ball BGA
  – 16mm x 12mm x 1.0 mm – 169-ball BGA
- **RoHS compliant**

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1 Product Description

1.1 General Description

Fortasa e•MMC products follow the JEDEC e•MMC 4.51 standard. It is an ideal universal storage solutions for many electronic devices, including smartphones, tablet PCs, PDAs, eBook readers, digital cameras, recorders, MP3, MP4 players, electronic learning products, digital TVs and set-top boxes. e•MMC integrates an e•MMC controller and MLC NAND in a JEDEC standard package. The e•MMC controller directly manages NAND flash, including ECC, wear-leveling, IOPS optimization and read sensing for reliable and predictable operation.

1.2. *e*MMC Standard Specification

The Fortasa e•MMC Device is fully compatible with the JEDEC Standard Specification No.JESD84-B4511. This datasheet describes the key and specific features of the Fortasa e•MMC Device. Any additional information required interfacing the Device to a host system and all the practical methods for device detection and access can be found in the proper sections of the JEDEC Standard Specification.

2 e•MMC Device and System

2.1 e•MMC System Overview

The Fortasa NAND Device contains a single chip MMC controller and NAND flash memory module. The Flash-controller interfaces with a host system allowing data to be written to and read from the NAND flash memory module. The controller makes all memory access completely transparent to the host..

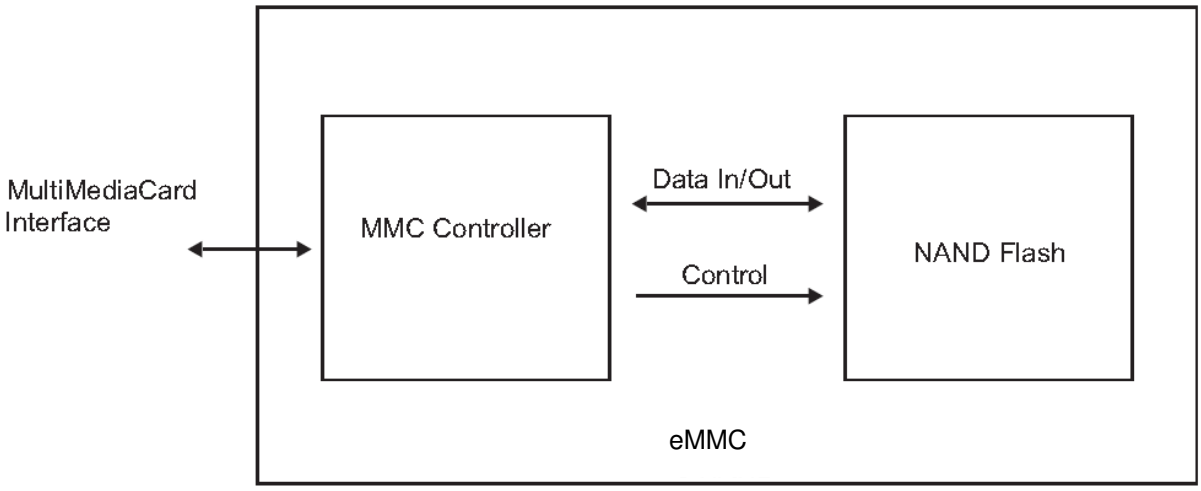


Figure 1: Functional block diagram

2.2. Memory Addressing

Previous implementations of the e•MMC specification (versions up to v4.1) are following byte addressing with 32 bit field. This addressing mechanism permitted for e•MMC densities up to and including 2 GB.

To support larger densities the addressing mechanism was update to support sector addresses (512B sectors). The sector addresses shall be used for all devices with capacity larger than 2 GB. To determine the addressing mode use the host should read bit [30:29] in the OCR register.

2.3. e•MMC Device Overview

The e•MMC device transfers data via a configurable number of data bus signals. The communication signals are:

2.3.1 Clock (CLK)

Each cycle of this signal directs a one bit transfer on the command and either a one bit (1x) or a two bits transfer (2x) on all the data lines. The frequency may vary between zero and the maximum clock frequency.

2.3.2 Command (CMD)

This signal is a bidirectional command channel used for Device initialization and transfer of commands. The CMD signal has two operation modes: open-drain for initialization mode, and push-pull for fast command transfer. Commands are sent from the e•MMC host controller to the e•MMC Device and responses are sent from the Device to the host.

2.3.3 Input/Outputs (DAT0-DAT7)

These are bidirectional data channels. The DAT signals operate in push-pull mode. Only the Device or the host is driving these signals at a time. By default, after power up or reset, only DAT0 is used for data transfer. A wider data bus can be configured for data transfer, using either DAT0-DAT3 or DAT0-DAT7, by the e•MMC host controller. The e•MMC Device includes internal pull-ups for data lines DAT1-DAT7. Immediately after entering the 4-bit mode, the Device disconnects the internal pull ups of lines DAT1, DAT2, and DAT3. Correspondingly, immediately after entering to the 8-bit mode the Device disconnects the internal pull-ups of lines DAT1–DAT7. The signals on the e•MMC interface are described in Table 4.

Table 4 – *e*•MMC Interface

Name	Type [1]	Description
CLK	I	Clock
DAT0	I/O/PP	Data
DAT1	I/O/PP	Data
DAT2	I/O/PP	Data
DAT3	I/O/PP	Data
DAT4	I/O/PP	Data
DAT5	I/O/PP	Data
DAT6	I/O/PP	Data
DAT7	I/O/PP	Data
CMD	I/O/PP/OD	Command/Response
RST_n	I	Hardware
VCC	S	Supply voltage for Core
VCCQ	S	Supply voltage for I/O
VSS	S	Supply voltage ground for Core
VSSQ	S	Supply voltage ground for I/O

Note I: input; O: output; PP: push-pull; OD: open-drain; NC: Not connected (or logical high); S: power supply.

Each Device has a set of information registers (see Section 4 - Device Registers.)

Table 5 – *e*•MMC Registers

Name	Width (Bytes)	Description	Description Implementation
CID	16	Device Identification number, an individual number for identification.	Mandatory
RCA	2	Relative Device Address, is the Device system address, dynamically assigned by the host during initialization.	Mandatory
DSR	2	Driver Stage Register, to configure the Device's output drivers.	Optional
CSD	16	Device Specific Data, information about the Device operation conditions.	Mandatory
OCR	4	Operation Conditions Register. Used by a special broadcast command to identify the voltage type of the Device.	Mandatory
EXT_CSD	512	Extended Device Specific Data. Contains information about the Device capabilities and selected modes. Introduced in standard v4.0	Mandatory

The host may reset the device by:

- Switching the power supply off and back on. The device shall have its own power-on detection circuitry which puts the device into a defined state after the power-on Device.
- A reset signal
- By sending a special command

2.4. Bus Protocol

After a power-on reset, the host must initialize the device by a special message-based *e*•MMC bus protocol. For more details, refer to section 5.3.1 of the JEDEC Standard Specification No.JESD84-B4511.

2.5. Bus Speed Modes

e•MMC defines several bus speed modes. **Table 6** summarizes the various modes.

Table 6— Bus Speed Modes

Model Name	Data Rate	IO Voltage	Bus Width	Frequency	Max Data Transfer (implies x8 bus width)
Backwards Compatibility with legacy MMC Card	Single	3.3/1.8V	1, 4, 8	0-26MHz	26MB/s
High Speed SDR	Single	3.3/1.8V	4, 8	0-52MHz	52MB/s
High Speed SDR	Dual	3.3/1.8V	4, 8	0-52MHz	104MB/s
HS200	Single	1.8V	4, 8	0-200MHz	200MB/s

2.5.1 HS200 Bus Speed Mode

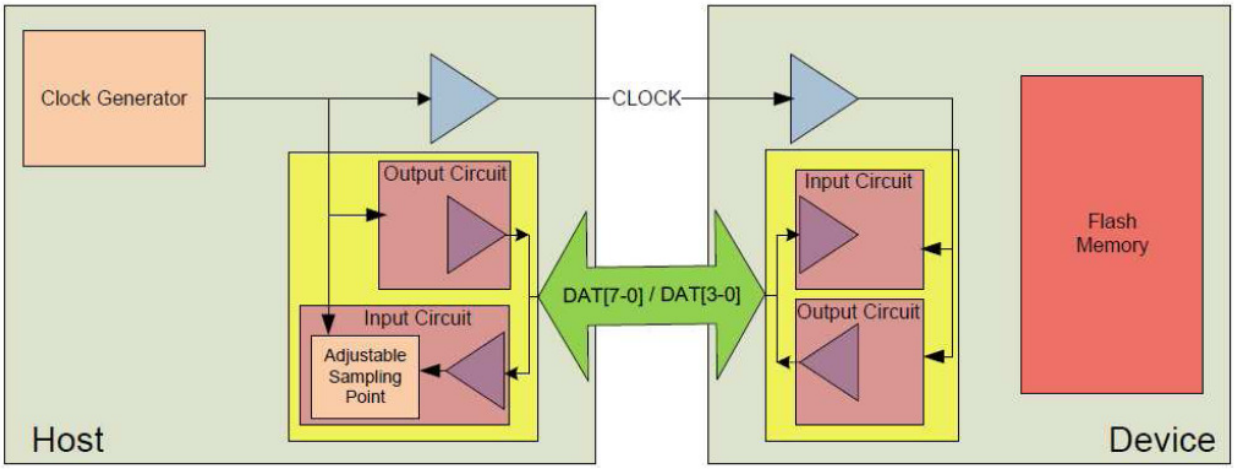
The HS200 mode offers the following features:

- SDR Data sampling method
- CLK frequency up to 200MHz Data rate – up to 200MB/s
- 4 or 8-bits bus width supported
- Single ended signaling with 4 selectable Drive Strength
- Signaling levels of 1.8V
- Tuning concept for Read Operations

2.5.2 HS200 System Block Diagram

Figure 2 shows a typical HS200 Host and Device system. The host has a clock generator, which supplies CLK to the Device. For write operations, clock and data direction are the same, write data can be transferred synchronous with CLK, regardless of transmission line delay. For read operations, clock and data direction are opposite; the read data received by Host is delayed by round-trip delay, output delay and latency of Host and Device. For reads, the Host needs to have an adjustable sampling point to reliably receive the incoming data.

Figure 2 — Host and Device Block Diagram



3. *e*•MMC Functional Description

3.1 *e*•MMC Overview

All communication between host and device are controlled by the host (master). The host sends a command, which results in a device response. For more details, refer to section 6.1 of the JEDEC Standard Specification No.JESD84-B451.
Five operation modes are defined for the *e*•MMC system (hosts and devices):

- Boot mode
- Device identification mode
- Interrupt mode
- Data transfer mode
- Inactive mode

3.2 Boot Operation Mode

In boot operation mode, the master (*e*•MMC host) can read boot data from the slave (*e*•MMC device) by keeping CMD line low or sending CMD0 with argument + 0xFFFFFFFA, before issuing CMD1. The data can be read from either boot area or user area depending on register setting. For more details, refer to section 6.3 of the JEDEC Standard Specification No.JESD84-B451.

3.3 Device Identification Mode

While in device identification mode the host resets the device , validates operation voltage range and access mode, identifies the device and assigns a Relative device Address (RCA) to the device on the bus. All data communication in the Device Identification Mode uses the command line (CMD) only. For more details, refer to section 6.4 of the JEDEC Standard Specification No.JESD84-B451.

3.4 Interrupt Mode

The interrupt mode on the *e*•MMC system enables the master (*e*•MMC host) to grant the transmission allowance to the slaves (Device) simultaneously. This mode reduces the polling load for the host and hence, the power consumption of the system, while maintaining adequate responsiveness of the host to a Device request for service. Supporting *e*•MMC interrupt mode is an option, both for the host and the Device. For more details, refer to section 6.5 of the JEDEC Standard Specification No.JESD84-B451.

3.5 Data Transfer Mode

When the Device is in *Stand-by* State, communication over the CMD and DAT lines will be performed in push-pull mode. For more details, refer to section 6.6 of the JEDEC Standard Specification No.JESD84-B451.

3.5.1 Data Read

The DAT0-DAT7 bus line levels are high when no data is transmitted. For more details, refer to section 6.6.9 of the JEDEC Standard Specification No.JESD84-B451.

3.5.2 Data Write

The data transfer format of write operation is similar to the data read. For more details, refer to section 6.6.10 of the JEDEC Standard Specification No.JESD84-B451.

3.5.3 Erase

In addition to the implicit erase executed by the Device as part of the write operation, provides a host explicit erase function. For more details, refer to section 6.6.11 of the JEDEC Standard Specification No.JESD84-B451.

3.5.4 TRIM
The TRIM operation is similar to the default erase operation described (See Section 6.6.12 of JESD84-B451). The TRIM function applies the erase operation to write blocks instead of erase groups. The TRIM function allows the host to identify data that is no longer required so that the Device can erase the data if necessary during background erase events. For more details, refer to section 6.6.12 of the JEDEC Standard Specification No.JESD84-B451.

3.5.5 Secure TRIM
The Secure Trim command is very similar to the Secure Erase command. The Secure Trim command performs a secure purge operation on write blocks instead of erase groups. To minimize the impact on the device's performance and reliability the Secure Trim operation is completed by executing two distinct steps.
For additional information please refer JESD84-B451 section number 6.6.16.

3.5.6 Sanitize
The Sanitize operation is a feature, in addition to TRIM and Erase that is used to remove data from the device. The use of the Sanitize operation requires the device to physically remove data from the unmapped user address space. For more details, refer to section 6.6.13 of the JEDEC Standard Specification No.JESD84-B451.

3.5.7 Discard
The Discard is similar operation to TRIM. The Discard function allows the host to identify data that is no longer required so that the device can erase the data if necessary during background erase events. For more details, refer to section 6.6.14 of the JEDEC Standard Specification No.JESD84-B451.

3.5.8 Write Protect Management
In order to allow the host to protect data against erase or write, the *e*•MMC shall support two levels of write protect commands. For more details, refer to section 6.6.15 of the JEDEC Standard Specification No.JESD84-B451.

3.5.9 Application-Specific Commands
The *e*•MMC system is designed to provide a standard interface for a variety applications types. In this environment, it is anticipated that there will be a need for specific customers/applications features. For more details, refer to section 6.6.17 of the JEDEC Standard Specification No.JESD84-B451.

3.5.10 Sleep (CMD5)
A Device may be switched between a Sleep state and a Standby state by SLEEP/AWAKE (CMD5). In the Sleep state the power consumption of the memory device is minimized. For more details, refer to section 6.6.18 of the JEDEC Standard Specification No.JESD84-B451.

3.5.11 Replay Protected Memory Block
A signed access to a Replay Protected Memory Block is provided. This function provides means for the system to store data to the specific memory area in an authenticated and replay protected manner. For more details, refer to section 6.6.19 of the JEDEC Standard Specification No.JESD84-B451.

3.5.12 Dual Data Rate Mode Selection
After the host verifies that the Device complies with version 4.4, or higher, of this standard, and supports dual data rate mode, it may enable the dual data rate data transfer mode in the Device. For more details, refer to section 6.6.20 of the JEDEC Standard Specification No.JESD84-B451.

3.5.13 Dual Data Rate Mode Operation
After the Device has been enabled for dual data rate operating mode, the block length parameter of CMD17, CMD18, CMD24, CMD25 and CMD56 automatically default to 512 bytes and cannot be changed by CMD16 (SET_BLOCKLEN) command which becomes illegal in this mode. For more details, refer to section 6.6.21 of the JEDEC Standard Specification No.JESD84-B451.

3.5.14 Background Operations
Devices have various maintenance operations need to perform internally. In order to reduce latencies during time critical operations like read and write, it is better to execute maintenance operations in other times – when the host is not being serviced. For more details, refer to section 6.6.22 of the JEDEC Standard Specification No.JESD84-B451.

3.5.15 High Priority Interrupt (HPI)
In some scenarios, different types of data on the device may have different priorities for the host. For example, writing operation may be time consuming and therefore there might be a need to suppress the writing to allow demand paging requests in order to launch a process when requested by the user. For more details, refer to section 6.6.23 of the JEDEC Standard Specification No.JESD84-B451.

3.5.16 Context Management
To better differentiate between large sequential operations and small random operations, and to improve multitasking support, contexts can be associated with groups of read or write commands. Associating a group of commands with a single context allows the device to optimize handling of the data. For more details, refer to section 6.6.24 of the JEDEC Standard Specification No.JESD84-B451.

3.5.17 Data Tag Mechanism
The mechanism permits the device to receive from the host information about specific data types (for instance file system metadata, time-stamps, configuration parameters, etc.). The information is conveyed before a write multiple blocks operation at well-defined addresses. By receiving this information the device can improve the access rate during the following read and update operations and offer a more reliable and robust storage. For more details, refer to section 6.6.25 of the JEDEC Standard Specification No.JESD84-B451.

3.5.18 Packed Commands
Read and write commands can be packed in groups of commands (either all read or all write) that transfer the data for all commands in the group in one transfer on the bus, to reduce overheads. For more details, refer to section 6.6.26 of the JEDEC Standard Specification No.JESD84-B451.

3.5.19 Real Time Clock Information
Providing real time clock information to the device may be useful for internal maintenance operations. Host may provide either absolute time (based on UTC) if available, or relative time. This feature provides a mechanism for the host to update both real time clock and relative time updates (see CMD49). For more details, refer to section 6.6.31 of the JEDEC Standard Specification No.JESD84-B451.

3.5.20 Power Off Notification
The host should notify the device before it powers the device off. This allows the device to better prepare itself for being powered off. For more details, refer to section 6.6.32 of the JEDEC Standard Specification No.JESD84-B451.

3.6 Inactive Mode
The device will enter inactive mode if either the device operating voltage range or access mode is not valid. The device can also enter inactive mode with GO_INACTIVE_STATE command (CMD15). The device will reset to *Pre-idle* state with power cycle. For more details, refer to section 6.1 of the JEDEC Standard Specification No.JESD84-B451.

3.7 Clock Control
The *e*•MMC bus clock signal can be used by the host to put the Device into energy saving mode, or to control the data flow (to avoid under-run or over-run conditions) on the bus. The host is allowed to lower the clock frequency or shut it down. For more details, refer to section 6.7 of the JEDEC Standard Specification No.JESD84-B451.

3.8 Error Conditions
Refer to section 6.8 of the JEDEC Standard Specification No.JESD84-B451.

3.9 Minimum Performance
Refer to section 6.9 of the JEDEC Standard Specification No.JESD84-B451.

3.10 Commands
Refer to section 6.10 of the JEDEC Standard Specification No.JESD84-B451.

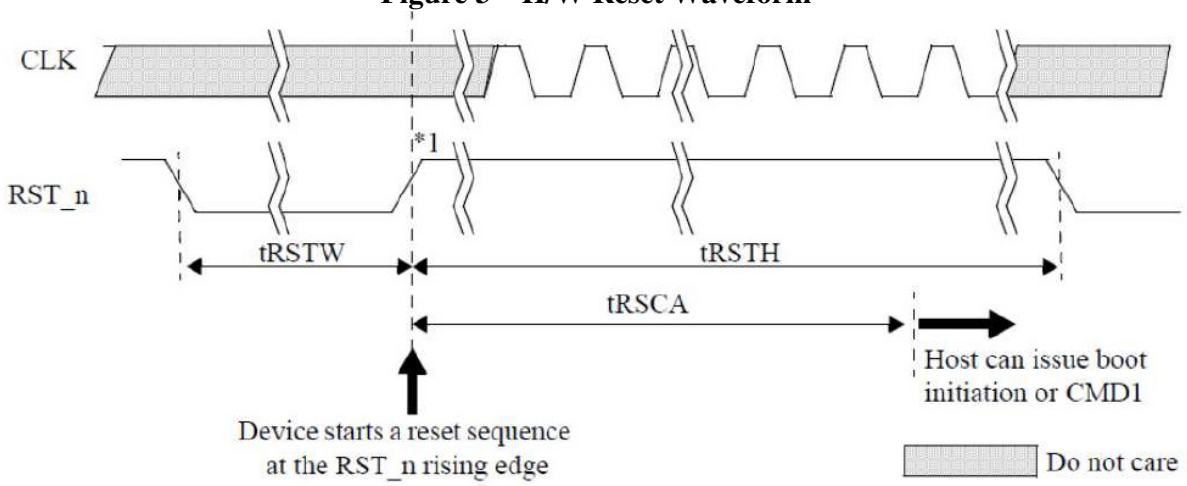
3.11 Device State Transition Table
Refer to section 6.11 of the JEDEC Standard Specification No.JESD84-B451.

3.12 Responses
Refer to section 6.12 of the JEDEC Standard Specification No.JESD84-B451.

3.13 Timings
Refer to section 6.15 of the JEDEC Standard Specification No.JESD84-B451.

3.14 H/W Reset Operation

Figure 3 – H/W Reset Waveform



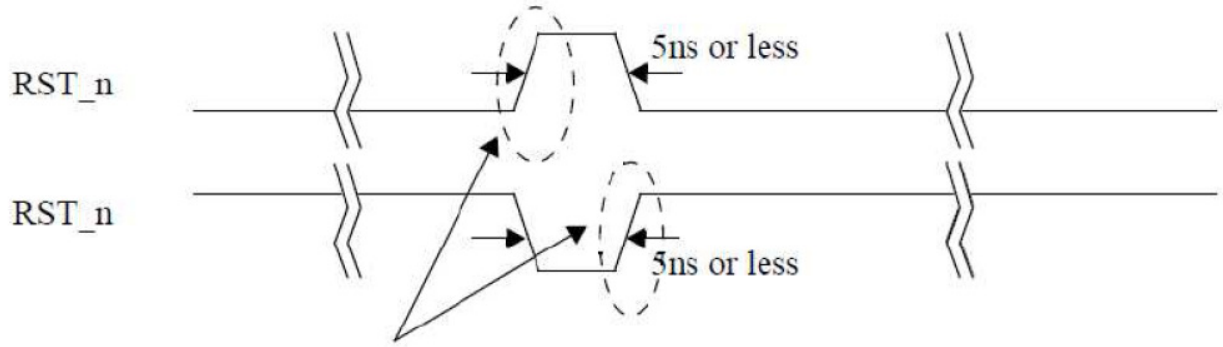
Note1: Device will detect the rising edge of RST_n signal to trigger internal reset sequence

Table 7 – H/W Reset Timing Parameters

Symbol	Comment	Min	Max	Unit
tRSTW	RST_n Pulse Width	1		µs
tRSCA	RST_n to Comand Line	200[1]		µs
tRSTH	RST_n high period (interval time)	1		µs
Note1 : 74 cycles of clock signal required before issuing CMD1 or CMD0 with argument 0xFFFFFFFA				

3.15 Noise Filtering Timing for H/W Reset

Device must filter out 5ns or less pulse width for noise immunity



Device must not detect these rising edge

Figure 4 – Noise Filtering Timing for H/W Reset

Device must not detect 5ns or less of positive or negative RST_n pulse. Device must detect more than or equal to 1us of positive or negative RST_n pulse width.

4. Device Registers

Within the Device interface six registers are defined: OCR, CID, CSD, EXT_CSD, RCA and DSR. These can be accessed only by corresponding commands (see Section 6.10 of JESD84-B451). The OCR, CID and CSD registers carry the Device/content specific information, while the RCA and DSR registers are configuration registers storing actual configuration parameters. The EXT_CSD register carries both, Device specific information and actual configuration parameters.

4.1. OCR Register

The 32-bit operation conditions register (OCR) stores the VDD voltage profile of the Device and the access mode indication. In addition, this register includes a status information bit. This status bit is set if the Device power up procedure has been finished. The OCR register shall be implemented by all Devices. For detailed register setting value, please refer to appendix or Fortasa FAE.

4.2. CID Register

The Card Identification (CID) register is 128 bits wide. It contains the Device identification information used during the Device identification phase (*e*•MMC protocol). For detailed register setting value, please refer to appendix or Fortasa FAE.

4.3. CSD Register

The Card-Specific Data (CSD) register provides information on how to access the Device contents. The CSD defines the data format, error correction type, maximum data access time, data transfer speed, whether the DSR register can be used etc. For detailed register setting value, please refer to appendix or Fortasa FAE.

4.4. Extended CSD Register

The Extended CSD register defines the Device properties and selected modes. It is 512 bytes long. The most significant 320 bytes are the Properties segment, which defines the Device capabilities and cannot be modified by the host. The lower 192 bytes are the Modes segment, which defines the configuration the Device is working in. These modes can be changed by the host by means of the SWITCH command. For detailed register setting value, please refer to appendix or Fortasa FAE.

4.5. RCA Register

The writable 16-bit Relative Device Address (RCA) register carries the Device address assigned by the host during the Device identification. This address is used for the addressed host-Device communication after the Device identification procedure. The default value of the RCA register is 0x0001. The value 0x0000 is reserved to set all Devices into the *Stand-by State* with CMD7. For detailed register setting value, please refer to appendix or Fortasa FAE.

4.6. DSR Register

The 16-bit driver stage register (DSR) is described in detail in Section 7.6 of the JEDEC Standard Specification No.JESD84-B451. It can be optionally used to improve the bus performance for extended operating conditions (depending on parameters like bus length, transfer rate or number of Devices). The CSD register carries the information about the DSR register usage. For detailed register setting value, please refer to appendix or Fortasa FAE.

5. The *e*•MMC bus

The *e*•MMC bus has ten communication lines and three power supply lines:

• **CMD**： Command is a bidirectional signal. The host and Device drivers are operating in two modes, open drain and push/pull.

• **DAT0-7**： Data lines are bidirectional signals. Host and Device drivers are operating in push-pull mode

• **CLK**： Clock is a host to Device signal. CLK operates in push-pull mode

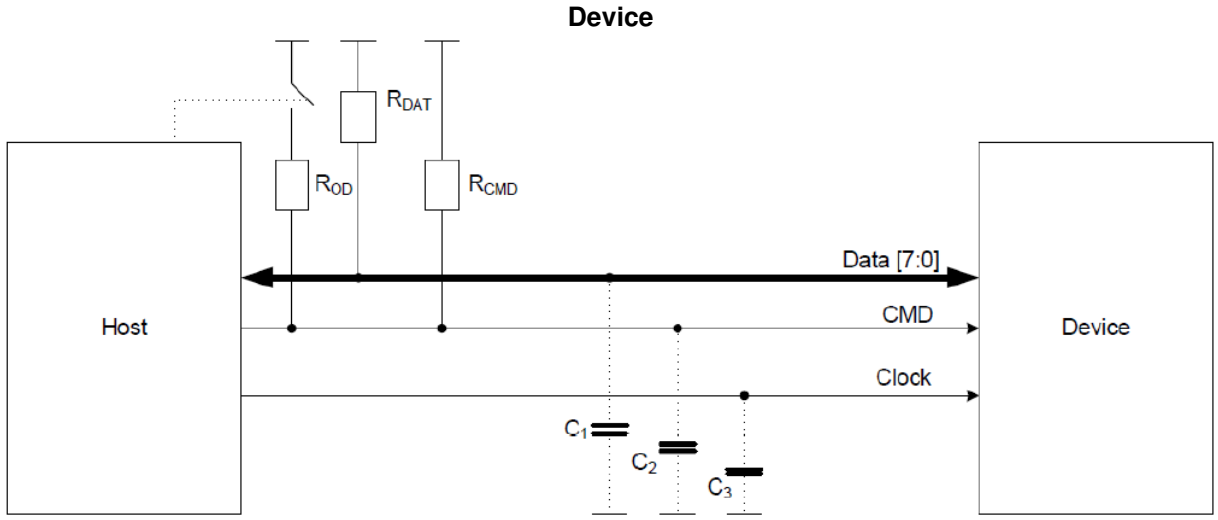


Figure 5 – Bus Circuitry Diagram

The R_{OD} is switched on and off by the host synchronously to the open-drain and push-pull mode transitions. The host does not have to have open drain drivers, but must recognize this mode to switch on the R_{OD}. R_{DAT} and R_{CMD} are pull-up resistors protecting the CMD and the DAT lines against bus floating device when all device drivers are in a high-impedance mode.

A constant current source can replace the R_{OD} by achieving a better performance (constant slopes for the signal rising and falling edges). If the host does not allow the switchable R_{OD} implementation, a fixed R_{CMD} can be used). Consequently the maximum operating frequency in the open drain mode has to be reduced if the used R_{CMD} value is higher than the minimal one given in Table 15.

5.1 Power-up

5.1.1 e•MMC power-up

An e•MMC bus power-up is handled locally in each device and in the bus master. Figure 6 shows the power-up sequence and is followed by specific instructions regarding the power-up sequence. Refer to section 10.1 of the JEDEC Standard Specification No.JESD84-B451 for specific instructions regarding the power-up sequence.

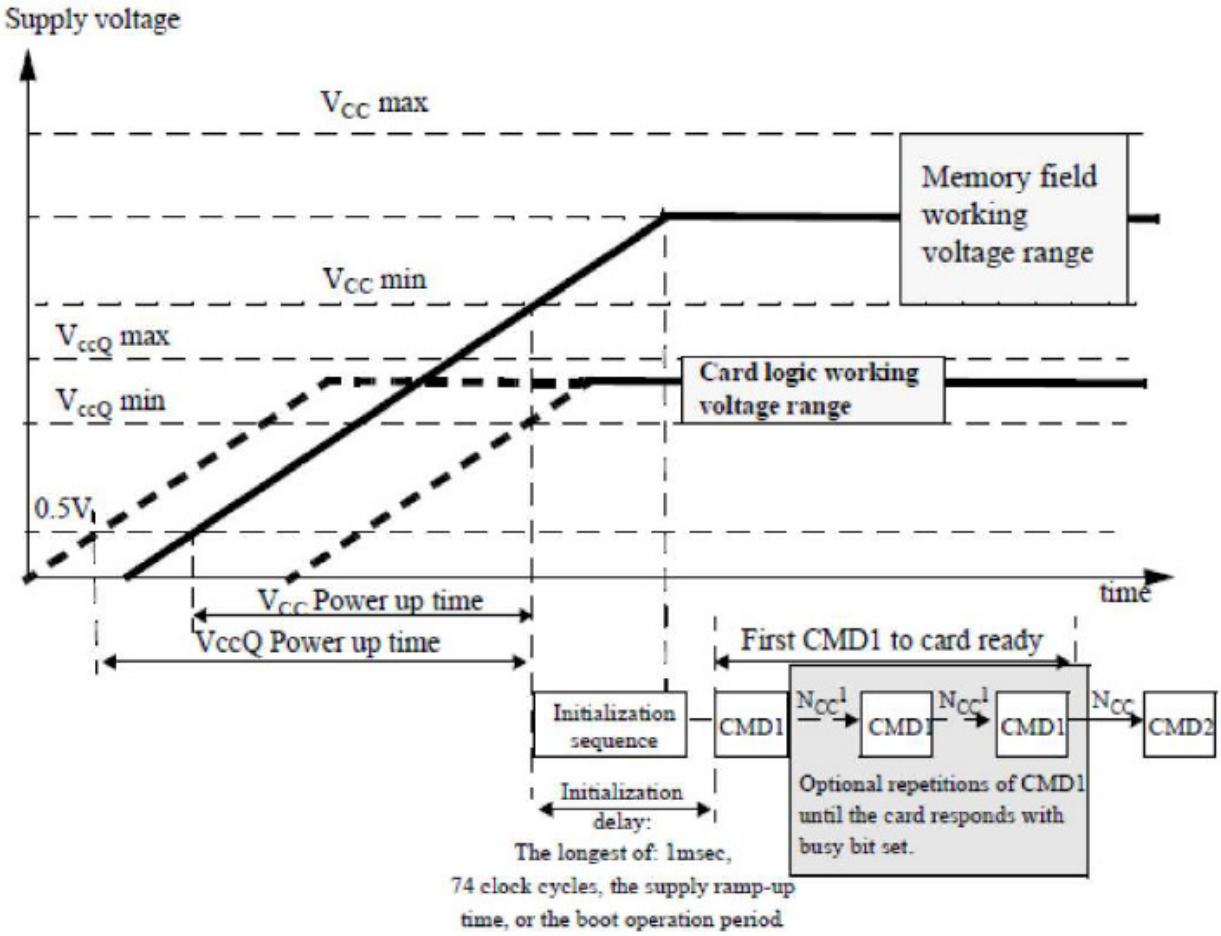


Figure 6 – e•MMC Power-up Diagram

5.1.2 e•MMC Power Cycling

The master can execute any sequence of V_{CC} and V_{CCQ} power-up/power-down. However, the master must not issue any commands until V_{CC} and V_{CCQ} are stable within each operating voltage range. After the slave enters sleep mode, the master can power-down V_{CC} to reduce power consumption. It is necessary for the slave to be ramped up to V_{CC} before the host issues CMD5 (SLEEP_AWAKE) to wake the slave unit. For more information about power cycling see Section 10.1.3 of the JEDEC Standard Specification No.JESD84-B451.

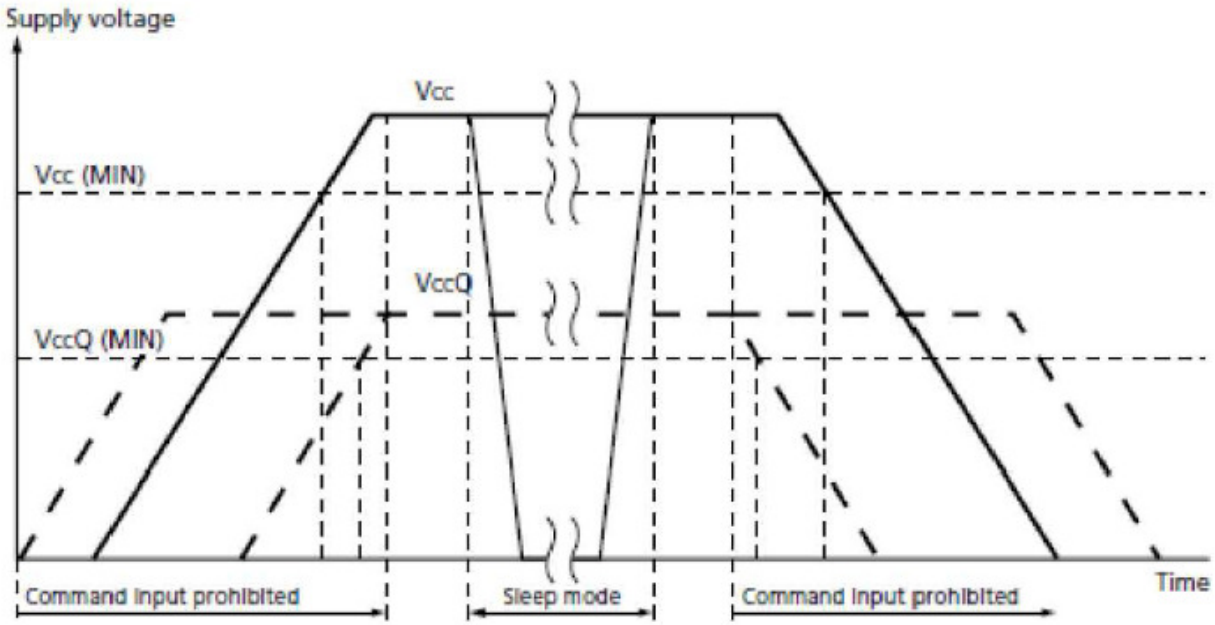


Figure 7 – The e•MMC Power Cycle

5.2 Bus Operating Conditions

Table 12 – General Operating Conditions

Parameter	Symbol	Min	Max	Unit
Peak voltage on all lines		-0.5	V_{CCQ} + 0.5	V
All Inputs				
Input Leakage Current (before initialization sequence and/or the internal pull-up resistor's connected)		-100	100	µA
Input Leakage Current (after initialization sequence and/or the internal pull-up resistor's connected)		-2	2	µA
All Outputs				
Output Leakage Current (before initialization sequence)		-100	100	µA
Output Leakage Current (after initialization sequence)		-2	2	µA
Note1 : initialization sequence is defined in section 10.1				

5.2.1 Power supply: e•MMC

In the e•MMC, V_{CC} is used for the NAND flash device and its interface voltage; V_{CCQ} is for the controller and the MMC interface voltage shown in Figure 8. The core regulator is optional and only required when internal core logic voltage is regulated from V_{CCQ}. A C_{Reg} capacitor must be connected to the V_{Ddi} terminal to stabilize regulator output on the system.

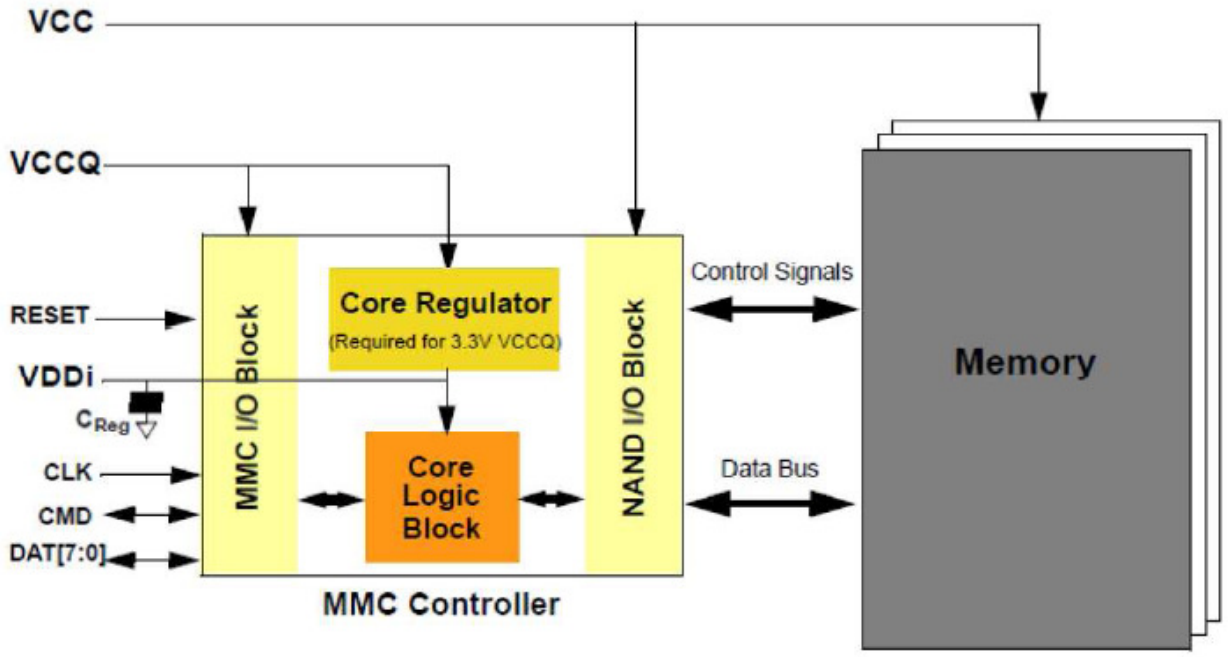


Figure 8 – *e*•MMC Internal Power Diagram

5.2.2 e•MMC Power Supply Voltage

The e•MMC supports one or more combinations of V_{CC} and V_{CCQ} as shown in Table 13. The V_{CCQ} must be defined at equal to or less than V_{CC}. The available voltage configuration is shown in Table 14.

Table 13 – *e*•MMC Power Supply Voltage

Parameter	Symbol	Min	Max	Unit
Supply Voltage (NAND)	V_{CC}	2.7	3.6	V
Supply Voltage (I/O)	V_{CCQ}	2.7	3.6	V
		1.65	1.95	V
Supply power-up for 3.3V	t_{PRUH}		3.5	ms
Supply power-up for 1.8V	t_{PRUL}		25	ms

The e•MMC must support at least one of the valid voltage configurations, and can optionally support all valid voltage configurations (see Table 14).

Table 14 – *e*•MMC Voltage Combinations

		V_{CCQ}	
		1.65V-1.95V	2.7V-3.6V[1]
V_{CC}	2.7V-3.6V	Valid	Valid
Note1 : VccQ (I/O) 3.3 volt range is not supported in HS200 devices			

6. Product Specification

6.1. System Performance

Table 15: Standard Performance specifications of e•MMC

Performance \ Capacity	4GB	8GB	16GB	32GB
Sustained read (MB/s)	29	29	29	29
Sustained write (MB/s)	11	11	21	32
Random Read (IOPS)	2100	2100	2700	2800
Random Write (IOPS)	270	230	400	420

Note 1: Values given for an 8-bit bus width, running HS200 mode from Fortasa developed tool, V_{CC}=3.3V, V_{CCQ}=3.3V.
Note 2: For performance number under other test conditions, please contact your Fortasa representatives.
Note 3: Performance numbers might be subject to changes without notice.

6.2 Power Consumption

Table 16 lists the e•MMC power consumption.

Table 16: e•MMC power consumption

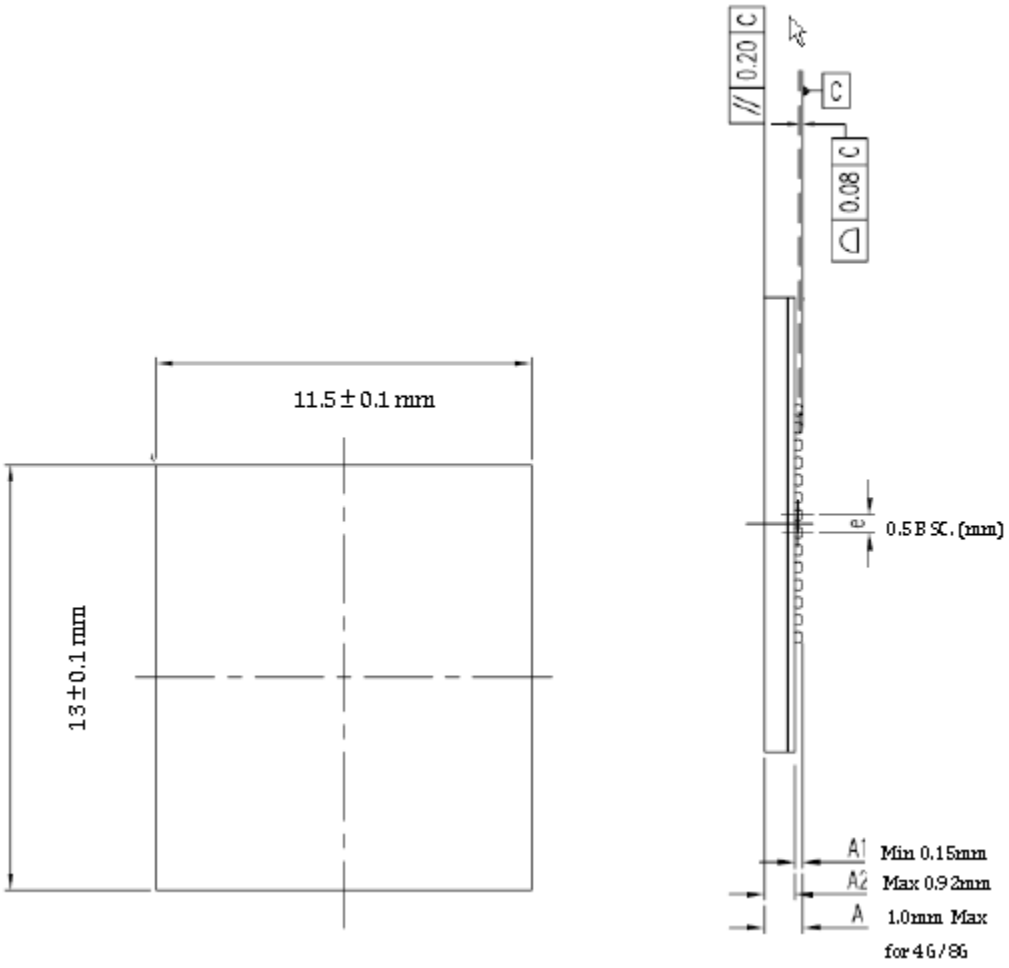
Performance \ Capacity	4GB	8GB	16GB	32GB	Condition
Read Mode (mA)	200	200	200	200	Typical
Write Mode (mA)	200	200	200	200	Typical
Standby Mode (µA)	270	270	285	300	Typical

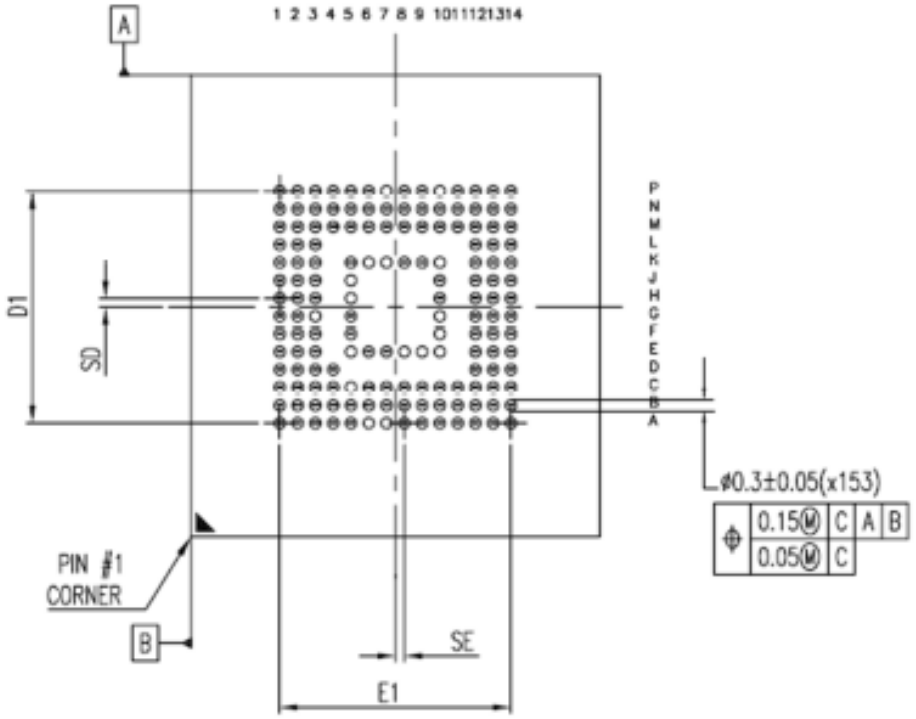
Note 1: Values given for an 8-bit bus width, a clock frequency of 52MHz DDR mode, V_{CC}= 3.3V±5%, V_{CCQ}=3.3V±5%
Note 2: Current numbers might be subject to changes without notice.

7. Package connections

7.1. Package Mechanical

153 ball FBGA (11.5 X 13.0 X 1.0mm for 4GB/8GB)

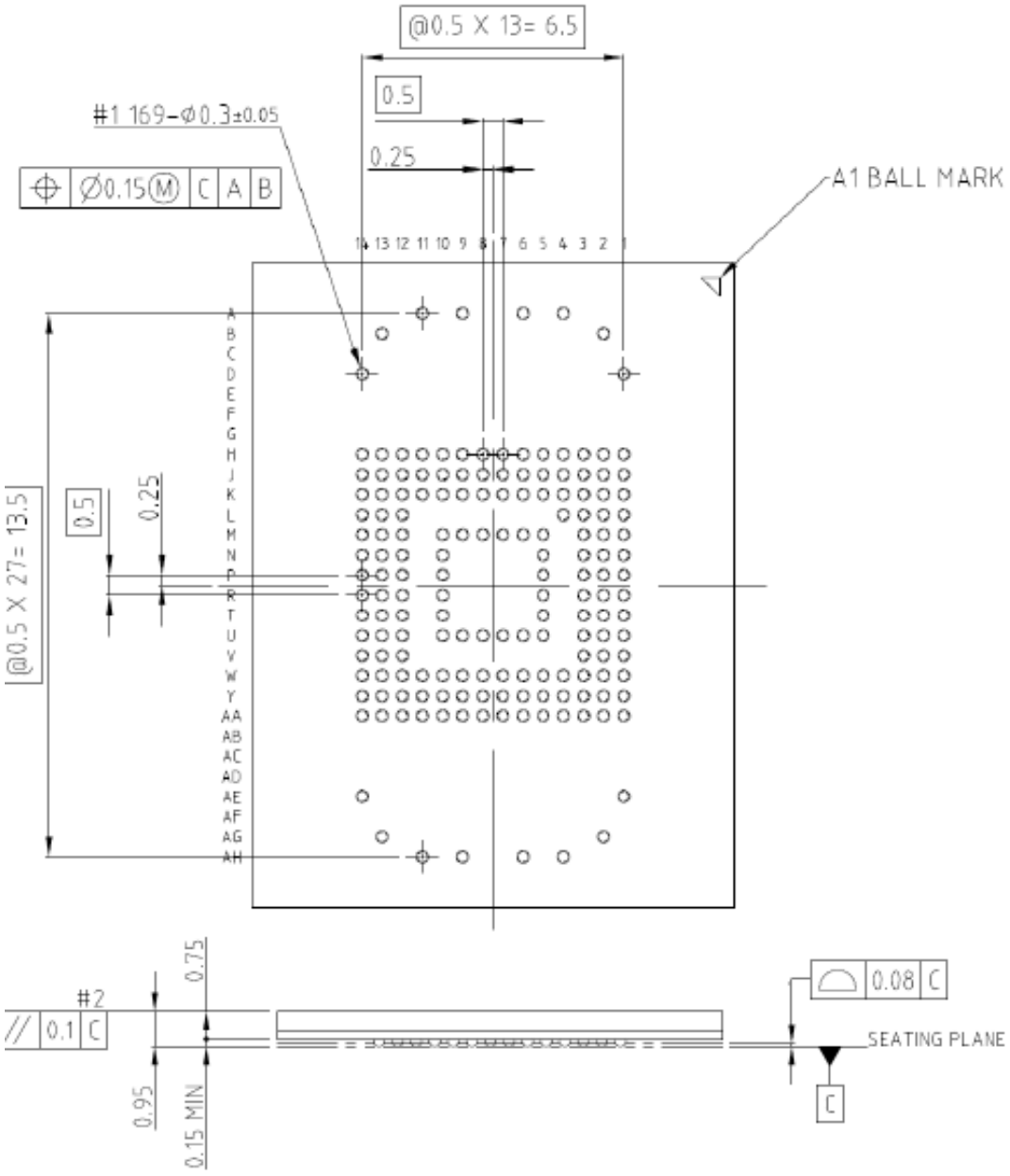


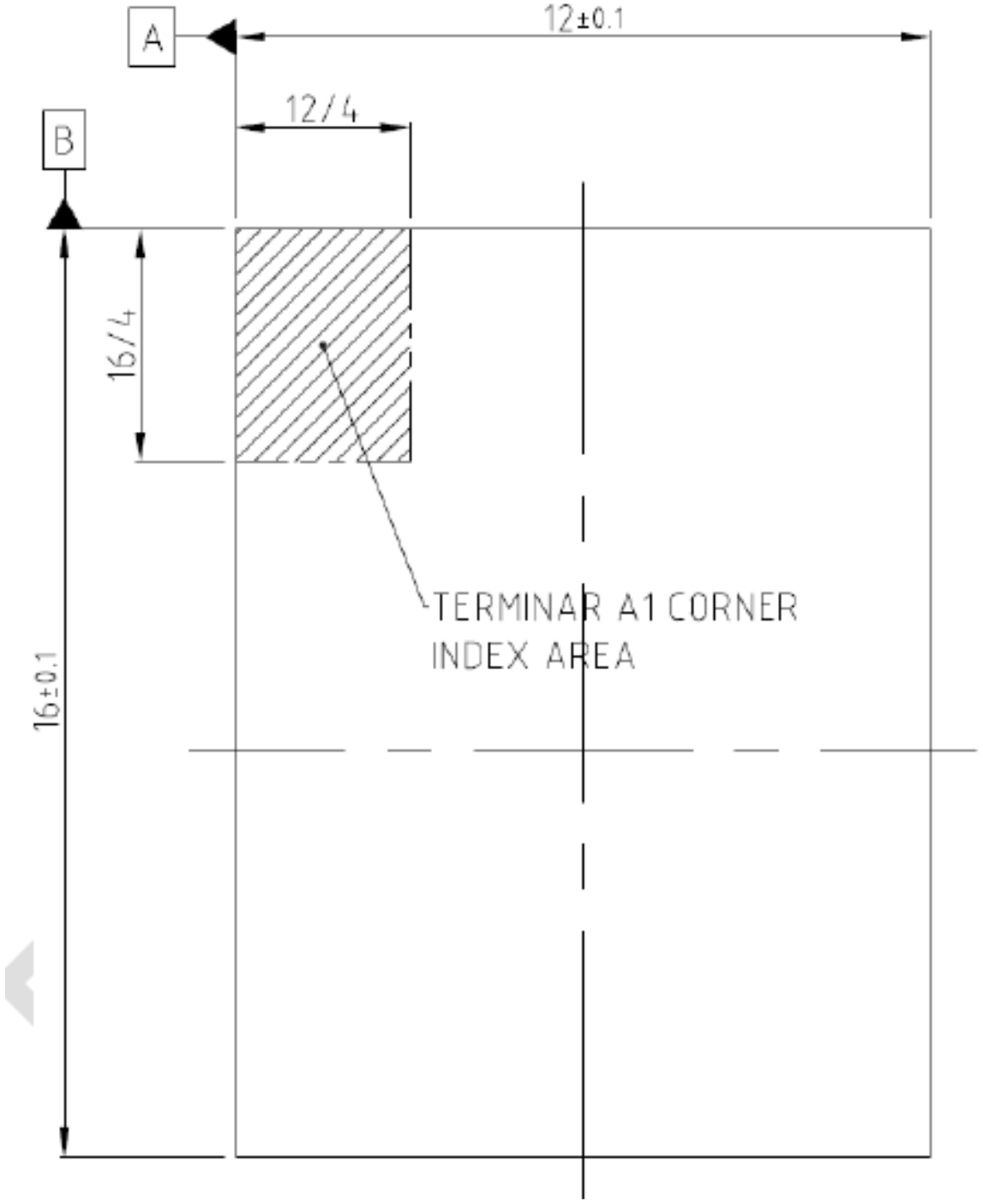


BOTTOM VIEW

N	SE (MM)	SD (MM)	E1(MM)	D1(MM)	JEDEC(REF)
153	0.25 BSC.	0.25 BSC.	6.50 BSC.	6.50 BSC.	MO-276 BA

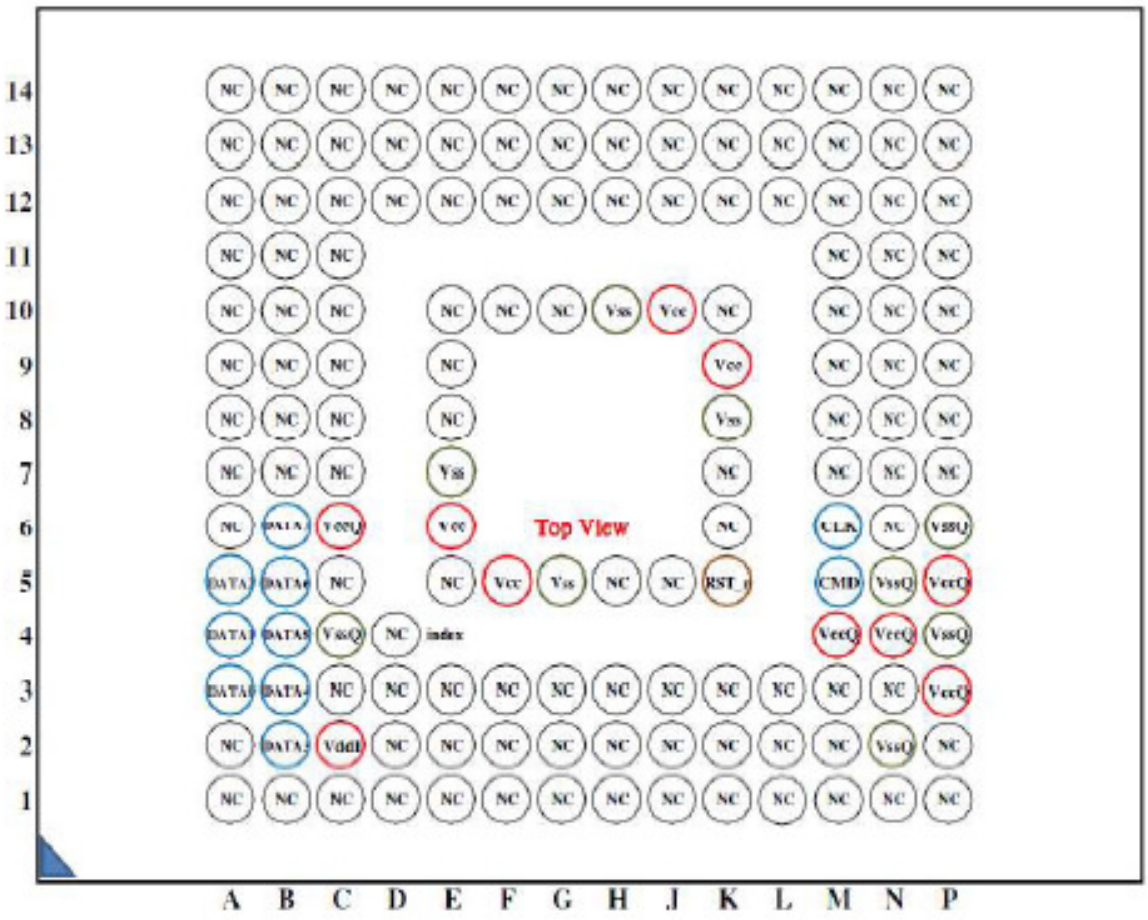
169 ball FBGA (16 X 12 X 1.0mm for 8GB/16GB/32GB)
Bottom and Side View



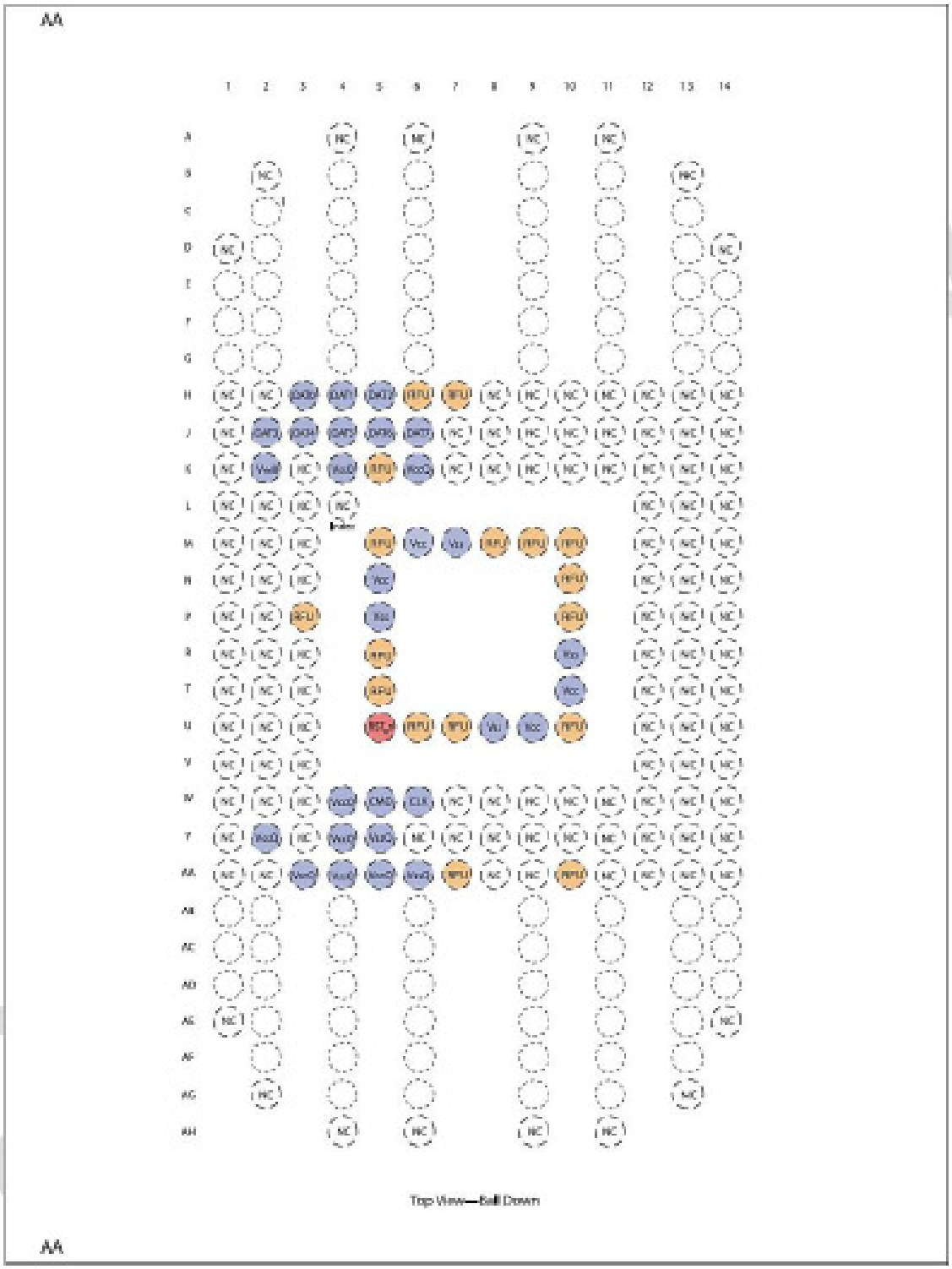

A
12±0.1
12/4
B
16/4
TERMINAR A1 CORNER
INDEX AREA
16±0.1

8. Ball Assignment

8.1. 153 ball assignment



8.2. 169 ball assignment

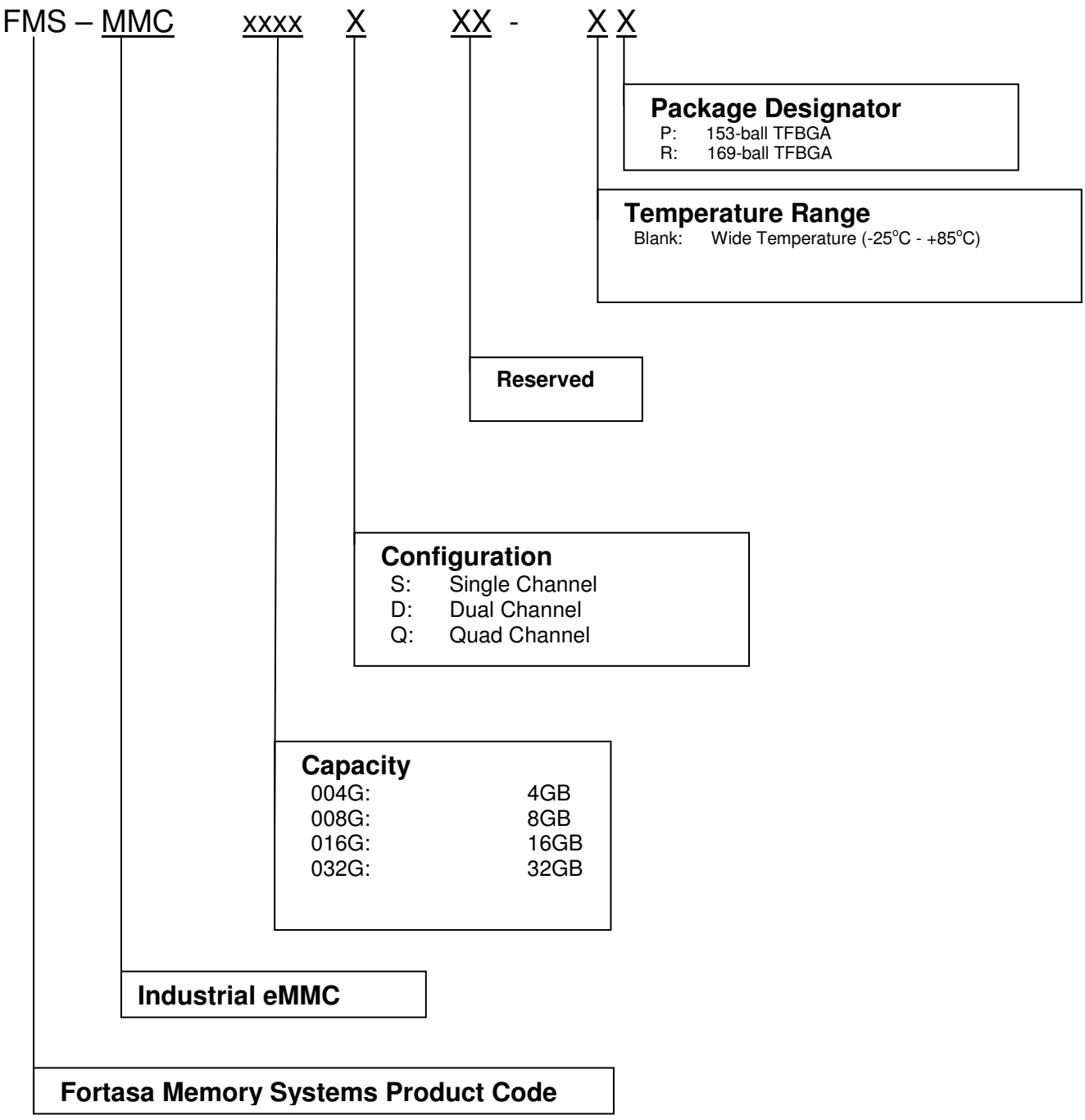


9. Ball Out and Signal Description

153-Ball Device	169-Ball Device	Symbol	Type	
M6	W6	CLK	Input	Clock: Each cycle directs a 1-bit transfer on the command and DAT lines.
M5	W5	CMD	Input	Command: A bidirectional channel used for device initialization Command has two operating mode : 1) Open-drain for initialization. 2) Push-pull for fast command transfer.
A3	H3	DAT0	I/O	Data I/O0: Bidirectional channel used for data transfer.
A4	H4	DAT1	I/O	Data I/O1: Bidirectional channel used for data transfer.
A5	H5	DAT2	I/O	Data I/O2: Bidirectional channel used for data transfer.
B2	J2	DAT3	I/O	Data I/O3: Bidirectional channel used for data transfer.
B3	J3	DAT4	I/O	Data I/O4: Bidirectional channel used for data transfer.
B4	J4	DAT5	I/O	Data I/O5: Bidirectional channel used for data transfer.
B5	J5	DAT6	I/O	Data I/O6: Bidirectional channel used for data transfer.
B6	J6	DAT7	I/O	Data I/O7: Bidirectional channel used for data transfer.
K5	U5	RST_n	Input	Reset signal pin
E6, F5, J10, K9	M6, N5, T10, U9	VCC	Supply	VCC: Flash memory I/F and Flash memory power supply.
C6, M4, N4, P3, P5	K6, W4, Y4, AA3, AA5	VccQ	Supply	VccQ: Memory controller core and MMC interface I/O power supply.
E7, G5, H10, K8	M7, P5, R10, U8	VSS	Supply	Vss: Flash memory I/F and Flash memory ground connection.
C4, N2, N5, P4, P6	K4, Y2, Y5, AA4, AA6	VssQ	Supply	VssQ
C2	K2	VDDi		VDDi : Connect 0.1uF capacitor from VDDi to ground.

10. Product Ordering Information

10.1 Product Code Designations



10.2 Valid Combinations

Capacity	Standard Temperature Model Numbers
4GB	FMS-MMC004GS1M-P
8GB	FMS-MMC008GD1M-P
8GB	FMS-MMC008GS1M-R
16GB	FMS-MMC008GD1M-R
32GB	FMS-MMC008GQ4M-R

Note: Valid combinations are those products in mass production or will be in mass production. Consult your Fortasa sales representative to confirm availability of valid combinations and to determine availability of new product combinations

11. Revision History

Revision	Date	Description	Comments
1.0	12/26/2013	Initial Preliminary Release	
1.1	4/17/2014	Integrate 20nm NAND Flash die. Updated performance and Power specs.	
1.2	6/12/2014	Updated 169-ball package and 16GB and 32GB offering.	